What is claimed is:

1. 1.     A wireless apparatus comprising:

2.     a forward error correction (FEC) coder to encode digital data using a low

3. density parity check (LDPC) code, said FEC coder including:

4.     a matrix multiplication unit to multiply input data by a transpose of a

5. first portion of a parity check matrix to generate modified data;

6.     a differential encoder to differentially encode said modified data to

7. generate coded data; and

8.     a concatenation unit to concatenate the input data and the coded data to

9. form a code word; and

10. a wireless transmitter to transmit a wireless signal that includes said code word.

1. 2.     The wireless apparatus of claim 1, wherein:

2.     said wireless signal is an orthogonal frequency division multiplexing (OFDM)

3. signal.

1. 3.     The wireless apparatus of claim 1, further comprising:

2.     a mapper, between said FEC coder and said wirelews transmitter, to map said

3. code word based on a predetermined modulation scheme; and

4.     an inverse discrete Fourier transform unit to convert mapped data from a

5. frequency domain representation to a time domain representation.

1. 4.     The wireless apparatus of claim 1, wherein:

2.     said parity check matrix is substantially as described in the list file of Appendix

3. A.

1. 5.     The wireless apparatus of claim 1, wherein:

2.     said parity check matrix is the same as the matrix described in the list file of

3. Appendix A.

1   6.      The wireless apparatus of claim 1, further comprising:

2          a storage medium to store a representation of at least said first portion of said

3   parity check matrix for use by said matrix multiplication unit.

1   7.      The wireless apparatus of claim 6, wherein:

2          said storage medium is operative to store a representation of the entire parity

3   check matrix.

1   8.      The wireless apparatus of claim 6, wherein:

2          said storage medium is operative to store a matrix that is substantially as

3   described in the list file of Appendix A.

1   9.      The wireless apparatus of claim 6, wherein:

2          said storage medium is operative to store a matrix that is a portion of a matrix

3   that is substantially as described in the list file of Appendix A, said portion of said

4   matrix being a portion having columns of weight 4.

1   10.    The wireless apparatus of claim 1, wherein:

2          said LDPC code is a (2000, 1600) bit-length code.

1   11.    The wireless apparatus of claim 1, wherein:

2          said wireless apparatus is a wireless user device for use in a wireless network.

1   12.    The wireless apparatus of claim 1, wherein:

2          said wireless apparatus is a wireless access point.

1   13.    The wireless apparatus of claim 1, wherein:

2          said wireless apparatus is a wireless network interface module.

1　14.　The wireless apparatus of claim 1, wherein:

2　　said wireless apparatus is an integrated circuit.


1　15.　A method comprising:

2　　matrix multiplying input data by a transpose of a first portion of a parity check

3　matrix;

4　　processing a result of said matrix multiplication using differential encoding to

5　generate coded data;

6　　concatenating said input data and said coded data to form a code word; and

7　　generating and transmitting a wireless signal that includes said code word.


1　16.　The method of claim 15, wherein:

2　　said wireless signal is an orthogonal frequency division multiplexing (OFDM)

3　signal.


1　17.　The method of claim 15, further comprising:

2　　accessing a storage medium storing a representation of at least a portion of said

3　parity check matrix before matrix multiplying.


1　18.　The method of claim 15, wherein:

2　　said parity check matrix is substantially as described in the list file of Appendix

3　A.


1　19.　The method of claim 15, wherein:

2　　said parity check matrix is the same as the matrix described in the list file of

3　Appendix A.


1　20.　The method of claim 15, wherein:

2　　said parity check matrix defines a (2000, 1600) bit-length LDPC code.

1    21.    The method of claim 15, wherein:

2         generating and transmitting a wireless signal includes mapping said code word

3    into modulation symbols and processing said modulation symbols using an inverse

4    discrete Fourier transform.


1    22.    An article comprising a machine readable storage medium having a

2    representation of at least a portion of a parity check matrix stored thereon, said parity

3    check matrix being substantially as described in the list file of Appendix A.


1    23.    The article of claim 22, wherein:

2         said machine readable storage medium has a representation of the entire parity

3    check matrix stored thereon.


1    24.    The article of claim 22, wherein:

2         said machine readable storage medium has a portion of said parity check matrix

3    stored thereon that includes all columns of weight 4.


1    25.    The article of claim 22, wherein:

2         said parity check matrix is the same as the matrix described in the list file of

3    Appendix A.


1    26.    The article of claim 22, wherein:

2         said parity check matrix defines a (2000, 1600) bit-length LDPC code.


1    27.    The article of claim 22, wherein:

2         said article includes a wireless communication device.

1    28.    The article of claim 22, wherein:

2        said article comprises only said machine readable storage medium.


1    29.    The article of claim 22, wherein:

2        said machine readable storage medium comprises at least one of the following: a

3    semiconductor memory, a read only memory (ROM), a random access memory

4    (RAM), an erasable programmable read only memory (EPROM), an electrically

5    erasable programmable read only memory (EEPROM), a flash memory, a magnetic

6    card, an optical card, a magnetic disk, an optical disk, a CD-ROM, and a magneto-

7    optical disk.


1    30.    A system comprising:

2        a forward error correction (FEC) coder to encode digital data using a low

3    density parity check (LDPC) code, said FEC coder including:

4            a matrix multiplication unit to multiply input data by a transpose of a

5        first portion of a parity check matrix to generate modified data;

6            a differential encoder to differentially encode said modified data to

7        generate coded data; and

8            a concatenation unit to concatenate the input data and the coded data to

9        form a code word;

10        a wireless transmitter to transmit a wireless signal that includes said code word;

11    and

12        at least one dipole antenna coupled to said wireless transmitter to facilitate

13    transmission of said wireless signal.


1    31.    The system of claim 30, wherein:

2        said wireless signal is an orthogonal frequency division multiplexing (OFDM)

3    signal.

1 32. The system of claim 30, further comprising:

2 a storage medium to store a representation of at least said first portion of said

3 parity check matrix for use by said matrix multiplication unit.

1 33. The system of claim 30, wherein:

2 said parity check matrix is substantially as described in the list file of Appendix

3 A.

1 34. An article comprising a storage medium having instructions stored thereon that,

2 when executed by a computing platform, operate to:

3 matrix multiply input data by a transpose of a first portion of a parity check

4 matrix;

5 process a result of said matrix multiplication using differential encoding to

6 generate coded data;

7 concatenate said input data and said coded data to form a code word; and

8 generate and transmit a wireless signal that includes said code word.

1 35. The article of claim 34, wherein:

2 said wireless signal is an orthogonal frequency division multiplexing (OFDM)

3 signal.

1 36. The article of claim 34, wherein said instructions, when executed by the

2 computing platform, further operate to:

3 access a storage medium having at least a portion of said parity check matrix

4 stored thereon before matrix multiplying.

1 37. The article of claim 34, wherein:

2 said parity check matrix is substantially as described in the list file of Appendix

3 A.

1  38.  The article of claim 34, wherein:

2      said parity check matrix defines a (2000, 1600) bit-length LDPC code.